

Efficient Method for the Capacitance Calculation of Circularly Symmetric Via in Multilayered Media

Faton Tefiku, *Member, IEEE*, and Eikichi Yamashita, *Fellow, IEEE*

Abstract—The equivalent capacitance produced by a circularly symmetric via connecting two microstrip lines on different planes is efficiently calculated by using the rectangular boundary division method. The calculation is carried out considering effects of inhomogeneous media within the line structures as well as the ground conductor thickness on the capacitance produced by a microstrip via. Computational results for various via geometries are presented and compared with presently available data.

I. INTRODUCTION

A VERTICAL pathway or a via is often used to connect two transmission lines residing in different substrate layers of a multilayered circuit board. As the simplest model for analysis, a via is represented by an equivalent circuit consisting of capacitors and inductors [1], [2].

The capacitance of a via in a multilayered dielectric medium greatly depends on the parameters of substrate layers, while the inductance can be computed as in the case of free space [1], [2]. The quasistatic analyses of various via geometries have been reported based on integral equation formulations [1]–[4]. In the above references, a via structure is assumed to reside in a homogeneous medium [2], [3] or in a dielectric substrate [1], [4]. In practical applications, however, these regions are layered media. Therefore, an efficient analysis method is proposed here for the capacitance of a circularly symmetric via in a multilayered substrate with embedded ground planes. The equivalent capacitances of two kinds of circularly symmetric microstrip vias are calculated: a cylindrical via connecting two microstrip lines located on different layers above the ground plane and a cylindrical via connecting two microstrip lines through a circular hole made in a ground plate.

The via structure to be analyzed here is a perfectly conducting circular cylinder that may have circular lips at its ends placed in a multilayered medium. The existence of the lines connected by the via are neglected in order to preserve the circular symmetry of the problem. We essentially employ the rectangular boundary division method in the circular cylindrical coordinates [5], [6]. It must be mentioned here that the method to treat complicated multilayered structures is simple and the conductor thickness can be easily taken into account.

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F. Tefiku is with Denki Kogyo Co., Ltd., Tokyo 100, Japan.
E. Yamashita is with the University of Electro-communications, Tokyo 182, Japan.
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II. METHOD OF ANALYSIS

The analysis procedure will be briefly explained for the cylindrical via through a hole made in a ground plate with arbitrary substrate layers above and below the ground plane. Fig. 1 shows the cross-section of a cylindrical via hole structure that is divided into five regions with rectangular boundaries.

The potential distribution, Φ_i ($i = 1, 2, 3, 4, 5$), should satisfy Laplace's equation in the cylindrical coordinates, (ρ, ϕ, z) , subject to the boundary conditions on both sides of the region i , which can be derived by the method of the separation of variables as

$$\begin{aligned} \Phi_i(\rho, z) = & \Phi_{i0}(\rho) + \sum_{n=1}^{\infty} \{A_{in} \sinh[k_{in}(z - z_i)] \\ & + B_{in} \cosh[k_{in}(z - z_i)]\} \\ & \cdot [J_0(k_{in}\rho) + C_{in}Y_0(k_{in}\rho)] \\ & (r_{i1} \leq \rho \leq r_{i2}; \quad z_{i1} \leq z \leq z_{i2}) \end{aligned} \quad (1)$$

where $r_{i1,2}$ and $z_{i1,2}$ are the radial and the axial wall coordinates, respectively, of a cylindrical tube representing the i th region, and z_i takes the value z_{i1} for $z \leq 0$ and the value z_{i2} for $z \geq 0$. k_{in} are the roots of the following equation:

$$J_0(k_{in}r_{i1})Y_0(k_{in}r_{i2}) - J_0(k_{in}r_{i2})Y_0(k_{in}r_{i1}) = 0. \quad (2)$$

C_{in} is given by

$$C_{in} = -\frac{J_0(k_{in}r_{i1})}{Y_0(k_{in}r_{i1})} = -\frac{J_0(k_{in}r_{i2})}{Y_0(k_{in}r_{i2})} \quad (3)$$

and J_0 and Y_0 denote the 0th order Bessel functions of the first and second kind, respectively. For the cases where the z -axis is included, only Bessel function of the first kind must be used and, therefore, $C_{1n} = C_{5n} = 0$. A_{in} and B_{in} ($i = 1, \dots, 5$) are unknown coefficients and $B_{1n} = B_{5n} = 0$ in order to satisfy the boundary conditions on the top and bottom conductor walls.

Φ_{i0} ($i = 1, \dots, 5$) are functions of the ρ coordinate only and are given as $\Phi_{10} = \Phi_{50} = 0$, $\Phi_{20} = \Phi_{40} = V_0 \cdot \ln(c/\rho)/\ln(c/r_v)$, $\Phi_{30} = V_0 \cdot \ln(r_g/\rho)/\ln(r_g/r_v)$, and V_0 is the given potential to the cylindrical conductor.

Next, we determine the total electric field energy in the structure from the above potential distributions and follow the procedure described in [6].

The other structure of a microstrip via to be analyzed with this method, a cylindrical via placed above a ground plane,

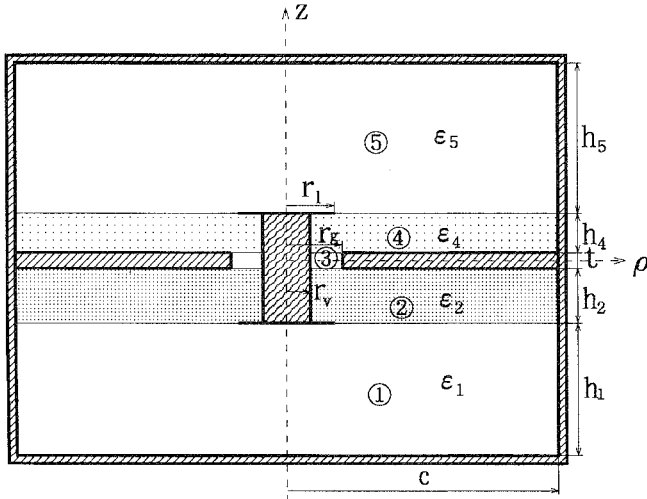


Fig. 1. Cross-section of a cylindrical via through a hole made in a ground plate.

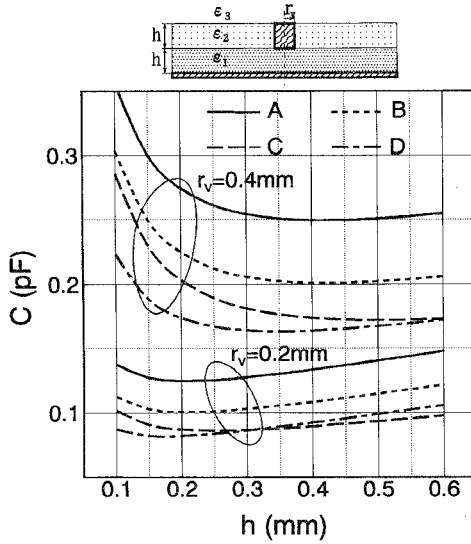


Fig. 2. Capacitance of a cylindrical via placed above a ground plane as a function of the cylinder height. (A) $\epsilon_{r1} = \epsilon_{r2} = \epsilon_{r3} = 4.0$, (B) $\epsilon_{r1} = \epsilon_{r2} = 4.0$, $\epsilon_{r3} = 1.0$, (C) $\epsilon_{r1} = 4.0$, $\epsilon_{r2} = 2.65$, $\epsilon_{r3} = 1.0$, and (D) $\epsilon_{r1} = 2.65$, $\epsilon_{r2} = 4.0$, $\epsilon_{r3} = 1.0$.

can be obtained from the one given in Fig. 1 by simply removing the center ground conductor and applying appropriate dimensions and permittivities for dielectric substrate layers. This problem requires only three divided subregions for the analysis.

III. NUMERICAL RESULTS

In Fig. 2, the capacitances of cylindrical vias placed above a ground conductor for the via radius of $r_v = 0.2$ mm and $r_v = 0.4$ mm are shown as a function of the cylinder height, h , for various combinations of dielectric substrate layers. Although the curves approximately show the same trend, numerical results indicate that the capacitance values are greatly different from case to case. When analyzing a via

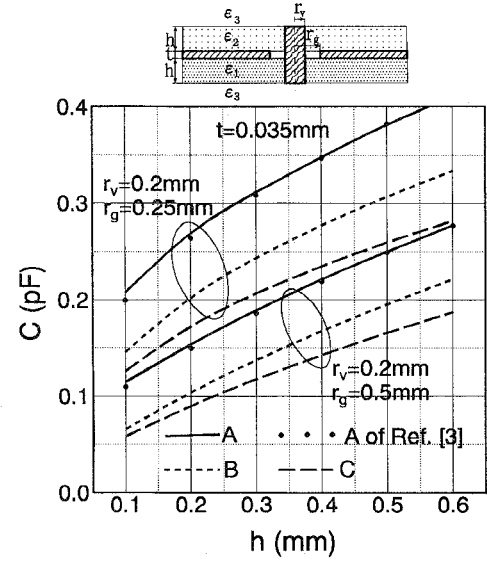


Fig. 3. Capacitance of a cylindrical via through a hole made in a ground plate as a function of the substrate height. (A) $\epsilon_{r1} = \epsilon_{r2} = \epsilon_{r3} = 4.0$, (B) $\epsilon_{r1} = \epsilon_{r2} = 4.0$, $\epsilon_{r3} = 1.0$, and (C) $\epsilon_{r1} = 4.0$, $\epsilon_{r2} = 2.65$, $\epsilon_{r3} = 1.0$.

structure in a dielectric substrate, represented by the curve B, one will obtain the capacitance values which differ for more than 20% from that of the via residing in a homogeneous medium, represented by the curve A.

The capacitance of the cylindrical via through a circular hole made in a ground plate as a function of the substrate height, h , for the via radius of $r_v = 0.2$ mm is shown in Fig. 3. For the case of a via structure residing in a homogeneous medium, curve A, our numerical results are in good agreement with the corresponding numerical results of [3], as can be seen in Fig. 3. Our results for the capacitance of a via structures in inhomogeneous media seems to be new. Typical computation time for one capacitance value is about 6 seconds on a HP-715 workstation. It has been found that calculated capacitance values of the curve A are higher than those of the curve B from 20–90%. This relative difference increases as the via height decreases or the ground plane opening increases. In other words, the difference is related to the amount of the electric field concentrated within the dielectric slab.

Next, we calculate the capacitance of a cylindrical via hole containing circular lips at its ends. Fig. 4 shows the via capacitance against the lip radius, r_l , for the via radius $r_v = 0.2$ mm, via height $h = 0.5$ mm, and ground plane opening $r_g = 0.4$ mm. The capacitances of the via hole in a dielectric substrate for four different permittivities have been presented and compared with the numerical results of [4]. Very good agreement between our numerical results and those reported in [4] is observed. In addition, we were able to calculate the capacitances of the via structures with different substrate layers above and below the ground plane.

IV. CONCLUSION

This letter article described a simple and efficient method to be used for the quasi-TEM wave analysis of circular cylindrical conductors in a multilayered medium. The method

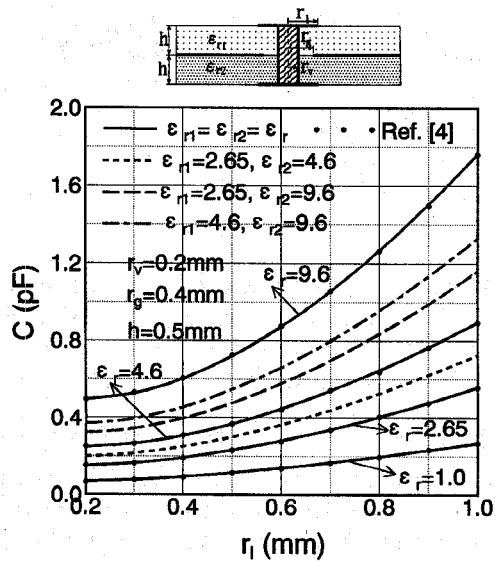


Fig. 4. Capacitance of a cylindrical via hole as a function of the lip radius.

is applied to the analysis of a circularly symmetric microstrip via placed above a ground plane or through a hole made in a

ground plane. The via capacitances of various geometries have been calculated with special attention to the inhomogeneity of the region in which the via resides. Numerical results clearly indicate that one must consider the inhomogeneity of the structure to obtain accurate prediction for the capacitance of a via.

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